CLAIMS

1. (currently amended) A method for detecting biphase encoded data comprising:

receiving a biphase encoded signal, the biphase encoded signal characterized as including unit bit cells each having a logic value encoded as a mid-symbol signal transition between a first half-symbol signal component and a second half-symbol signal component;

~~demodulating~~ integrating the first half-symbol signal component of a unit bit cell over a half-symbol period to produce a first half-signal component value and integrating the second half-symbol signal component[[s]] of a unit bit cell over a half-symbol period to produce a second half-signal component value; and

generating a difference signal corresponding to the difference between the ~~demodulated~~ integrated values of the first and second half-symbol components, such that the difference signal may be utilized to determine the logic value of the unit bit cell.

2. (original) The method of claim 1, further comprising detecting the logic value of the received unit bit cell by comparing the difference signal with a validity threshold value.

3. (original) The method of claim 1, wherein the received biphase encoded signal is a Manchester encoded signal.

4. (original) The method of claim 1, wherein said biphase encoded signal is modulated as amplitude shift keyed, frequency shift keyed, or phase shift keyed.

5. (currently amended) The method of claim 1, wherein said step of generating a difference signal comprises subtracting the ~~demodulated~~ integrated first half-symbol signal component value from the ~~demodulated~~ integrated second half-symbol signal component value.

6. (currently amended) The method of claim 1, wherein said step of generating a difference signal comprises subtracting the ~~demodulated~~ integrated second half-symbol signal component value from the ~~demodulated~~ integrated first half-symbol signal component value.

7. (currently amended) The method of claim 1, further comprising the step of ~~said demodulating step comprising~~ demodulating the first and second half-symbol signal components of the unit bit cell over sequential half symbol clock periods.

8. (currently amended) The method of claim 1, ~~wherein said demodulating step~~ further comprising the step of correlating the first and second half-symbol signal components of the unit bit cell.

9. (original) The method of claim 8, wherein said correlating step comprises separating the first and second half-symbol signal components of the unit bit cell.

10. (canceled)

11. (currently amended) A biphase code ~~detector for detecting biphase encoded data comprising: a~~ receiver that receives a biphase encoded signal, wherein the biphase encoded signal is characterized as including unit bit cells each having a logic value encoded as a mid-symbol transition between a first half-symbol signal component and a second half-symbol signal component;

the receiver comprising:

~~a demodulator that demodulates~~ first and second integrator and dump devices, the first integrator and dump device integrating the first half-symbol component of a unit bit cell over a half-symbol period to produce a first half-signal component value and the second integrator and dump device integrating the second half-symbol component[[s]] of a unit bit cell over a half-symbol period to produce a second dhaf-symbol component value; and

a half-symbol differentiator that generates a difference signal corresponding to the difference between the ~~demodulated~~ integrated values of the first and second half-symbol components, such that the difference signal may be utilized to determine the logic value of the unit bit cell.

12. (currently amended) The receiver ~~system~~ of claim 11, further comprising an output detector that compares the difference signal with a validity threshold value to determine the logic value of the received unit bit cell.

13. (currently amended) The receiver ~~system~~ of claim 11, wherein said half-symbol differentiator comprises a subtractor.

14. (currently amended) The receiver ~~system~~ of claim 11, ~~said demodulator~~ further comprising means for correlating the first and second half-symbol components over sequential half-symbol clock periods.

15. (canceled)

16. (currently amended)The receiver ~~system~~ of claim 15, wherein said correlation means further comprises:

means for separating and passing the first half-symbol component ~~to either the first or second integrate and dump circuit;~~ and

~~means for separating and passing~~ the second half-symbol component ~~to the other of the first or second integrate and dump circuits~~.

17. (currently amended) The receiver ~~system~~ of claim 16, wherein said means for separating and passing comprise correlation multipliers.